Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) [A] An electronic computer comprising; a processing device including reconfigurable hardware that can create a logic circuit with a program, and a control device executing a command specified by the processing device, wherein said command is instructed to be executed when the processing device detects a predetermined condition and includes a command for execution of switching programs logically creating the reconfigurable hardware.

2. (Currently Amended) The electronic computer as defined in claim 1 wherein said processing device comprises a plurality of banks each having a processing element with reconfigurable hardware and at least one program data memory each holding a program that creates a logic circuit in said reconfigurable hardware, and an effective bank selection unit selecting one bank from the plurality of banks, making it effective and connecting it to the outside.

3. (Currently Amended) The electronic computer as defined in claim 1 wherein said processing device comprises a bank including a processing element that includes reconfigurable hardware, a plurality of program data memories each holding a program that creates a logic circuit in said reconfigurable hardware, and an effective block selection unit selecting one memory from the plurality of program data memories and making it effective.

4. (Currently Amended) The electronic computer as defined in claim 2 [or 3] wherein at least one processing element of said processing device is comprised of reconfigurable hardware and the other processing elements are each comprised of reconfigurable hardware or a general-purpose CPU.

5. (Currently Amended) The electronic computer as defined in claim 2~~, 3, or 4~~ wherein said control device interprets and executes;

an activate command specifying said effective bank in case where there is a plurality of said banks, and specifying said effective program data memory and activating operation of said specified processing element when there is a plurality of said program data memories;

a halt command halting operation of said specified processing device;

an interrupt command issuing an interrupt vector from said control device to said specified processing device;

a load_prg command transferring program data from a specified memory device to said program data memory;

a cancel_prg command canceling the load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

6. (Currently Amended) The electronic computer as defined in claim 1~~, 2, 3, 4 or 5~~ comprising a command code memory holding commands that said control device executes, wherein said control device comprises a command code reference device reading commands from the command code memory according to an address specified by said processing device, interpreting, and executing it.

7. (Original) The electronic computer as defined in claim 6 wherein said command code reference device comprises an address counter holding the address of said command code memory, and in the exchange of commands between said processing device and said control device, a first address control line indicating that an address signal line outputted by said processing device is effective, and a second address counter control line instructing whether the value of the address signal line is stored in the address counter as it is or the result of adding the value of the address signal line to the value of the address counter is stored in the address counter when the first control line is effective.

8. (Original) The electronic computer as defined in claim 7 wherein said commands are stored in said command code memory in a format comprising a command code that classifies the commands, an address counter control code, and a flag that indicates whether or not the following command is executed, and said address counter control code includes a load_adr command setting the value of the address counter and a add_adr command adding a specified value to the address counter.

9. (Original) The electronic computer as defined in claim 8 wherein said address counter control code includes a push_adr command that hides the address counter in an address counter stack provided in said control device and that sets a new value to the address counter, and a pop_adr command that returns the value of the address counter stack to the address counter.

10. (Currently Amended) The electronic computer as defined in ~~any of claims 1 to 9~~ claim 1 comprising a cache device including a cache memory that temporarily holds data to be transferred to said processing device and a cache controller that controls the cache memory wherein the cache controller is controlled by a command issued by said processing device.

11. (Original) The electronic computer as defined in claim 10 wherein said cache device comprises an address translation device that translates an address defined externally to said processing device into an address defined inside of the processing device, and the address translation device is controlled by a command issued by said processing device.

12. (Original) An electronic computer comprising; a processing device including reconfigurable hardware that can create a logic circuit with a program, and a control device executing a command specified by the processing device;

wherein said command is instructed to be executed when the processing device detects a predetermined condition and includes a command for execution of switching programs logically creating the reconfigurable hardware; and

said processing device comprises a second processing device including reconfigurable hardware that can create a logic circuit with a program and a second control device executing a command specified by the second processing device.

13. (Currently Amended) A semiconductor integrated circuit implementing the electronic computer as defined in claim 1 ~~any of claims 1 to 11~~.

14. (Currently Amended) A control method comprising [the steps of];

issuing an instruction to execute a command when a processing device including reconfigurable hardware that can create a logic circuit with a program detects a predetermined condition; and

executing switching programs that logically create reconfigurable hardware by a control device that has received the command execution instruction from the processing device.

15. (Original) The control method as defined in claim 14 wherein, after said switching, while a program in a predetermined program data memory is being executed, a next program is read into another program data memory.

16. (Currently Amended) A control method comprising ~~the steps of~~;

issuing an instruction to execute a command when a processing device detects a predetermined condition said processing device including reconfigurable hardware, a plurality of program data memories that hold programs creating logic circuits of the reconfigurable hardware, and an effective block selection unit that selects one program data memory from the plurality of program data memories and that makes it effective;

executing, by a control device that has received the command execution instruction from the processing device an activate command controlling the effective block selection unit so as to make a specified program data memory effective and connecting it to the reconfigurable hardware; and

switching the content of a logic circuit executed by the reconfigurable hardware.

17. (Original) The control method as defined in claim 16 wherein said control device execute;

a halt command halting the operation of said specified processing device;

an interrupt command issuing an interrupt vector from said control device to said specified processing device;

a load_prg command transferring program data from a specified memory device to said program data memory;

a cancel_prg command canceling the load_prg instruction, and

a wait_prg command waiting until the completion of the load_prg instruction.

18. (Original) A program generation method comprising;

a control flow analysis procedure in which the control flow of an application program is analyzed, the application program is divided into processing units, and a command sequence intermediate code combining commands controlled by reconfigurable hardware that executes the divided processing units within an electronic computer is generated;

a command sequence implementation procedure in which a command sequences is generated by translating the command sequence intermediate code into a form that can be executed by the electronic computer; and

a program data generation procedure in which the operational content of a processing unit is translated into a form that can be executed by the electronic computer.

19. (Original) The program generation method as defined in claim 18 wherein the application program is divided so that each processing unit can be stored in a program data memory that holds a program creating a logic of said reconfigurable hardware when the control flow of the application program is analyzed and divided into processing units in said control flow analysis procedure.

20. (Original) A program having a computer execute a procedure in which, when a processing device including reconfigurable hardware that can create a logic circuit with a program detects a predetermined condition and issues an instruction to execute a command, a control device that has received the command execution instruction from the processing device executes switching programs logically creating the reconfigurable hardware.

21. (Original) A program having a computer execute a procedure in which, when a processing device including reconfigurable hardware, a plurality of program data memories that hold programs creating logic circuits of the reconfigurable hardware, and an effective block selection unit that selects one program data memory from the plurality of program data memories and that makes it effective detects a predetermined condition and issues an instruction to execute a command, a control device that has received the command execution instruction from the processing device executes an activate command that controls the

effective block selection unit so as to make the specified program data memory effective and that switches connection to the reconfigurable hardware.

22. (Original) The program as defined in claim 21 having a computer execute a procedure in which a halt command halting operation of said specified processing device, an interrupt command issuing an interrupt vector from said control device to said specified processing device, a load_prg command transferring program data from a specified memory device to said program data memory, a cancel_prg command canceling the load_prg instruction, and a wait_prg command waiting until the completion of the load_prg instruction are executed.